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EXAMINER

ALHJIA, SAIF A

ART UNIT

PAPER NUMBER

2128

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/618,284	Applicant(s) BROOKES ET AL.	
	Examiner SAIF A. ALHIJA	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,5-16,18,19 and 24-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,5-16,18,19 and 24-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2128

DETAILED ACTION

1. Claims 1, 5-16, 18-19, and 24-36 have been presented for examination.

Claims 2-4, 17, and 20-23 have been cancelled.

Claims 34-36 are newly presented.

Response to Arguments

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2 May 2008 has been entered.

PRIOR ART ARGUMENTS

i) Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

EXAMINERS NOTE

ii) Examiner has cited particular columns and line numbers in the references applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

iii) The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution.

iv) Further, the Examiner respectfully encourages Applicants to direct the specificity of their response with regards to this office action to the broadest reasonable interpretation of the claims as presented. This will avoid issues that would delay prosecution such as limitations not explicitly presented in the claims, intended use statements that carry no patentable weight, mere allegations of patentability, and novelty that is not clearly expressed.

Art Unit: 2128

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 5-16, 18-19, and 24-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kim et al. "Combined Data-Driven and Event-Driven Scheduling Technique for Fast Distributed Cosimulation"**, hereafter **Kim** in view of **Ghosh et al. "A Hardware-Software Co-simulator for Embedded System Design and Debugging"**, hereafter **Ghosh**.

Regarding Claim 1:

The reference discloses A method in a host machine for validating a design for a system which comprises a software element, and first and second hardware components, the software element being for execution on the second hardware component, and the first and second hardware components being operable to interact with one another, the method comprising the steps of:

Art Unit: 2128

simulating operation of the first hardware component in a first software simulation system; **(Kim. Figure 5, HW)**

simulating the software element and the second hardware component in a second software simulation system; **(Kim. Figure 5, SW)**

receiving a variable synchronization parameter; **(Kim. Section III, paragraph 4, “In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.”)**

running the second software simulation system asynchronously with, and ahead of, the first software simulation system, wherein the second software simulation system advances at most by a number of processor cycles set in the variable synchronization parameter, the variable synchronization parameter limiting a maximum number of processor clock periods of the second simulation per period of a reference clock of the host machine; **(Kim. Section III, paragraph 4, “In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.”)**

controlling the first software simulation system using the second software simulation system that is running ahead of the first software simulation system, a socket allowing for communication between the second software simulation system and the first software simulation system; and **(Kim. Abstract, “intersimulator communications”)**

wherein the first software simulation system and the second software simulation system are implemented in separate processing threads within the host machine providing more rapid simulation of software instructions in the second software simulation system than the simulation of instructions in the first software simulation system. **(Kim. Section B, Paragraph 2,” The first three sets have a single task graph and the next three sets have two disconnected task graphs. Tasks mapped to the SW component are simulated sequentially in an SW simulator, while we use a separate HW simulator process for each task mapped to the HW component.)**

Kim does not explicitly recite analyzing a result from the first and second software simulation systems and validating the design for the system,

However Ghosh discloses analyzing a result from the first and second software simulation systems and validating the design for the system. (**Ghosh. Page 156, Bottom Right, “to provide adequate debugging capability for both hardware and software” and “to provide means for evaluation of performance metrics.”**)

Kim does not explicitly recite threads but rather recites tasks. Ghosh further discloses separate processing threads within the host machine (**Ghosh, Page 157, top right, "The co-simulator is implemented as a multithreaded program to allow easy integration of stand alone simulators."**)

Kim and Ghosh are analogous art in Hardware Software CoSimulation.

It would have been obvious to one of ordinary skill in the art at the time of invention to analyze and validate as per **Ghosh** the simulation of **Kim** in order to determine if the resultant design is working correctly and further with respect to threads see citation of Ghosh Page 157 top right.

Regarding Claim 5:

The reference discloses A method as claimed in claim 1, further comprising:

performing operations in the first software simulation system to set up an inter-process communications protocol connection therein; (**Kim. Abstract, “intersimulator communications”**)

connecting the second software simulation system to the interprocess communications protocol connection in the first software simulation system; (**Kim. Abstract, “intersimulator communications”**)

Kim does not explicitly recite connecting a software debugger to the second software simulation system; and controlling the first software simulation system from the software debugger via the second software simulation system using the interprocess communications protocol.

However Ghosh discloses connecting a software debugger to the second software simulation system; (**Ghosh. Abstract, "debugging software"**)

and controlling the first software simulation system from the software debugger via the second software simulation system using the interprocess communications protocol. (**Ghosh. Abstract, "debugging software"**)

Art Unit: 2128

It would have been obvious to one of ordinary skill in the art at the time of invention to debug as per **Ghosh** the simulation of **Kim** in order to determine if the resultant design is working correctly.

Regarding Claim 6:

The reference discloses A method as claimed in claim 1, further comprising:

performing operations in the first software simulation system to set up an inter-process communications protocol connection therein; (**Kim. Abstract, "intersimulator communications"**)

Kim does not explicitly recite connecting a software debugger to the communications protocol connection;

and controlling the first software simulation system from the software debugger using the inter-process communications protocol.

However Ghosh discloses connecting a software debugger to the communications protocol connection; (**Ghosh. Abstract, "debugging software"**)

and controlling the first software simulation system from the software debugger using the inter-process communications protocol. (**Ghosh. Abstract, "debugging software"**)

It would have been obvious to one of ordinary skill in the art at the time of invention to debug as per **Ghosh** the simulation of **Kim** in order to determine if the resultant design is working correctly.

Regarding Claim 7:

The reference discloses A method as claimed in claim 5 or 6, wherein the inter-process communications protocol is TCP/IP and the connection is a TCP/IP socket. (**Kim. Section VI-C, TCP/IP**)

Regarding Claim 8:

The reference discloses A method as claimed claim 1, wherein the second hardware component includes a processor. (**Kim. Section I, "programmable processors"**) (**Ghosh. Abstract, "processors"**)

Art Unit: 2128

Regarding Claim 9:

The reference discloses A method as claimed in claim 8, wherein the processor is an embedded processor.
(Kim. “embedded system design”) (Ghosh. Section 2, “embedded processor”)

Regarding Claim 10:

The reference discloses A method as claimed in claim 1, wherein the hardware component includes processor peripheral devices. **(Kim. Section I, “programmable processors”) (Ghosh. Abstract, “processors”)**

Regarding Claim 11:

The reference discloses A method as claimed in claim 10, wherein the peripheral devices are embedded.
(Kim. “embedded system design”) (Ghosh. Section 2, “embedded processor”)

Regarding Claim 12:

Kim does not explicitly recite A method as claimed in claim 1, wherein the first software simulation system is implemented using a hardware description language (HDL) simulation environment.

However, Ghosh discloses method as claimed in claim 1, wherein the first software simulation system is implemented using a hardware description language (HDL) simulation environment. **(Ghosh, Page 157, top left, “Verilog”)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize HDL as disclosed in Ghosh for the simulation in Kim since HDL is well known method for programming hardware.

Regarding Claim 13:

Kim does not explicitly recite A method as claimed in claim 1, wherein the second simulation is implemented using a C model.

However, Ghosh discloses A method as claimed in claim 1, wherein the second simulation is implemented using a C model. **(Ghosh, Page 161, top right “written in C”)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize C as disclosed in Ghosh for the simulation in Kim since C is well known programming language.

Regarding Claim 14:

The reference discloses A method as claimed in claim 1, wherein the first hardware component is a programmable logic device. **(Kim. Section I, “programmable processors”) (Ghosh. Introduction, Paragraph 2, “FPGA”)**

Regarding Claim 15:

The reference discloses A method in a hardware environment for controlling a simulation of a system using a software debugger, the simulation useful for validating a design of the system wherein the system comprises a software element, and first and second hardware components, the software element being for execution on the second hardware component and the first and second hardware components being operable to interact with one another, the method comprising the steps of:

simulating the first hardware component in a first software simulation in the hardware environment; **(Kim. Figure 5, HW)**

simulating the software element and the second hardware component in a second software simulation using a software model embedded within the hardware environment, the first software simulation and the second software simulation being implemented in separate processing threads within the hardware environment; **(Kim. Figure 5, SW)**

performing operations to set up an inter-process communications protocol connection; **(Kim. Abstract, “intersimulator communications”)**

receiving a variable synchronization parameter; **(Kim. Section III, paragraph 4, “In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.)**

running the second software simulation asynchronously with, and ahead of, the first software simulation, wherein the second software simulation advances at most by a number of processor clock cycles set in the variable

Art Unit: 2128

synchronization parameter, the variable synchronization parameter limiting a maximum number of processor clock periods of the second simulation per period of a reference clock of the hardware environment; (**Kim. Section III, paragraph 4, “In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.)**

controlling the first software simulation of the hardware component from the software debugger through the second software simulation using the inter-process communications protocol; (**Kim. Abstract, “intersimulator communications”) and**

Kim does not explicitly recite validating the design of the system using the first and second software simulations

and connecting the software debugger to the software model of the second software simulation embedded in the hardware environment;

However Ghosh discloses validating the design of the system using the first and second software simulations. (**Ghosh. Page 156, Bottom Right, “to provide adequate debugging capability for both hardware and software” and “to provide means for evaluation of performance metrics.”)**

and connecting the software debugger to the software model of the second software simulation embedded in the hardware environment; (**Ghosh. Abstract, "debugging software")**

Kim does not explicitly recite threads but rather recites tasks. Ghosh further discloses separate processing threads within the host machine (**Ghosh, Page 157, top right, "The co-simulator is implemented as a multithreaded program to allow easy integration of stand alone simulators.”)**

Kim and Ghosh are analogous art in Hardware Software CoSimulation.

It would have been obvious to one of ordinary skill in the art at the time of invention to debug, analyze, and validate as per **Ghosh** the simulation of **Kim** in order to determine if the resultant design is working correctly and further with respect to threads see citation of Ghosh Page 157 top right.

Regarding Claim 16:

The reference discloses A method as claimed in claim 15, further comprising the step of:

Art Unit: 2128

connecting the software debugger to inter-process communications protocol connection. **(Kim. Abstract, “intersimulator communications”)** **(Ghosh. Page 156, bottom left, “distributed communicating processes”)**

Regarding Claim 18:

The reference discloses A method as claimed in claim 15, wherein the inter-process communications protocol is TCP/IP and the connection is a TCP/IP socket. **(Kim. Section VI-C, TCP/IP)**

Regarding Claim 19:

The reference discloses A method as claimed in claim 15, wherein the step of simulating the second hardware component comprises simulating a processor and one or more peripheral devices with which the one or more processors interact directly. **(Kim. Section I, “programmable processors”)** **(Ghosh. Abstract, “processors”)**

Regarding Claim 24:

The reference discloses A method as claimed in claim 15, wherein the second hardware component includes embedded processors. **(Kim. “embedded system design”)** **(Ghosh. Section 2, “embedded processor”)**

Regarding Claim 25:

The reference discloses A method as claimed in claim 15, wherein the second hardware component includes embedded peripheral devices. **(Kim. “embedded system design”)** **(Ghosh. Section 2, “embedded processor”)**

Regarding Claim 26:

Kim does not explicitly recite A method as claimed in claim 15, wherein the first simulation is implemented using a hardware description language (HDL) simulation environment.

However Ghosh discloses A method as claimed in claim 15, wherein the first simulation is implemented using a hardware description language (HDL) simulation environment. **(Ghosh, Page 157, top left, “Verilog”)**

Art Unit: 2128

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize HDL as disclosed in Ghosh for the simulation in Kim since HDL is well known method for programming hardware.

Regarding Claim 27:

Kim does not explicitly recite A method as claimed in claim 15, wherein the second simulation is implemented using a C model.

However Ghosh discloses A method as claimed in claim 15, wherein the second simulation is implemented using a C model. **(Ghosh, Page 161, top right “written in C”)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize C as disclosed in Ghosh for the simulation in Kim since C is well known programming language.

Regarding Claim 28:

The reference discloses A method as claimed in claim 15, wherein the first hardware component is a programmable logic device. **(Kim. Section I, “programmable processors”) (Ghosh. Introduction, Paragraph 2, “FPGA”)**

Regarding Claim 29:

The reference discloses A method for providing an I/O interface for a simulation model to allow the simulation of interactive programs in a hardware environment for use in system validation, the method comprising:

simulating a software element in a first software simulation using a software model in a first processing thread in the hardware environment; **(Kim. Figure 5, SW)**

simulating an embedded input/output device within the simulation model in a second software simulation to produce an input/output device model in a second processing thread, the first software simulation running ahead of the second software simulation **(Kim. Section B, Paragraph 2,” The first three sets have a single task graph and the next three sets have two disconnected task graphs. Tasks mapped to the SW component are simulated sequentially in an SW simulator, while we use a separate HW simulator process for each task mapped to the**

Art Unit: 2128

HW component.) the first and second software simulations being synchronized using a reference clock parameter that limits a maximum number of processor clock periods of the first processing thread per period of a reference clock in the hardware environment, wherein the reference clock parameter is selectable; **(Kim. Section III, paragraph 4, “In the centralized approach, the central controller manages the component simulators with the information on how far the local clock of the simulator can advance.)**

connecting the input/output device model to a terminal emulator using an inter-process communications protocol; **(Kim. Abstract, “intersimulator communications”)**

polling the input/output device model for the transferred information using the software model. **(Kim. Section V, paragraph 4, “polling scheme”)**

Kim does not explicitly recite running an interactive program in the terminal emulator to transfer information to the input/output device model **(Kim discloses the transfer for information as per the Abstract, “intersimulator communications”), and**

validating the design of the system.

However Ghosh discloses running an interactive program in the terminal emulator to transfer information to the input/output device model, **(Ghosh. Section 3.3, “human interaction with the system being simulated.”)** and

validating the design of the system. **(Ghosh. Page 156, Bottom Right, “to provide adequate debugging capability for both hardware and software” and “to provide means for evaluation of performance metrics.”)**

Kim does not explicitly recite threads but rather recites tasks. Ghosh further discloses separate processing threads within the host machine **(Ghosh, Page 157, top right, “The co-simulator is implemented as a multithreaded program to allow easy integration of stand alone simulators.”)**

Kim and Ghosh are analogous art in Hardware Software CoSimulation.

It would have been obvious to one of ordinary skill in the art at the time of invention to provide an interface, analyze and validate as per **Ghosh** the simulation of **Kim** in order to determine if the resultant design is working correctly and further with respect to threads see citation of Ghosh Page 157 top right.

Art Unit: 2128

Regarding Claim 30:

The reference discloses A method as claimed in claim 29, the method further comprising: providing separate processing threads for the embedded input/output device to allow concurrent user inputs and outputs. **(Kim, Section IV-A, paragraph 2, "hardware component where block can be executed concurrently.") (Ghosh, Page 161, bottom right, "it was shown that suppression of periodic signals during concurrent fault simulation can produce significant savings in simulation time.")**

Regarding Claim 31:

The reference discloses A method as claimed in claim 29, wherein the inter-process communications protocol is TCP/IP. **(Kim, Section VI-C, TCP/IP)**

Regarding Claim 32:

Kim does not explicitly recite A method as claimed in claim 29, wherein the input/output device is a UART device.

However Ghosh discloses A method as claimed in claim 29, wherein the input/output device is a UART device. **(Ghosh, Figure 1, UART Simulator)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a UART device as in Ghosh in the simulation of Kim since UART is a well known communication device.

Regarding Claim 33:

Kim and Ghosh do not explicitly recite A method as claimed in claim 29, wherein the input/output device is an Ethernet MAC device.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize an Ethernet MAC device since it is a well known communications device.

Regarding Claim 34:

Kim and Ghosh do not explicitly recite that host machine comprises a plurality of processors.

Art Unit: 2128

However it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a plurality of processors since as per **Kim, Section VII** the cosimulation is distributed and can be performed at multiple geographic locations which implies multiple processors and further **Ghosh on page 156 right**, discusses the simulation of multiple processors. Further multiple processors are a well known method of making good use of hardware resources and increasing speed by dividing up the work amongst multiple processors.

Regarding Claim 35:

The reference discloses The method as claimed in claim 34, the method further comprising: setting a first software simulation variable, wherein the setting specifies synchronous or asynchronous simulation between the first software simulation system and the second software simulation system. (**Kim, Section IV-A, “Virtual Synchronization”**)

Regarding Claim 36:

The reference discloses The method as claimed in claim 35, wherein asynchronous simulation uses thread scheduling of the host machine. (**Kim, Figure 3, SW/HW Scheduling. Section B, Paragraph 2,” The first three sets have a single task graph and the next three sets have two disconnected task graphs. Tasks mapped to the SW component are simulated sequentially in an SW simulator, while we use a separate HW simulator process for each task mapped to the HW component.**)

Conclusion

4. All Claims are rejected.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAIF A. ALHIJA whose telephone number is (571)272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Art Unit: 2128

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

SAA

June 21, 2008